**ABSTRACT**

This paper proposes an innovative approach to address the increasing demand for high-performance, energy-efficient electronic devices. Nowadays, there is a greater demand for integrated circuits that provide top-notch performance, use less power, and remain cost-effective. Our project's aim is to create and implement a low power decoder, which is an important part of modern integrated circuits. Our main goal is to enhance the decoder's design to decrease power usage while maintaining top-notch performance and scalability. To achieve this objective, we explore various VLSI design styles, including CMOS, Transmission Gate Logic (TGL), Pass-transistor Dual-Value Logic (PDVL), and Gate Diffusion Input (GDI). Each of these methodologies present unique advantages in terms of power efficiency, speed, and area utilization.

Here the proposed GDI based logic decoder significantly decreases the transistor’s count that results in low power consumption. The spread of Cadence (Virtuoso) simulation at 90nm is used for implementing this proposed GDI decoder at with different various supply voltages, which shows reduction in power dissipation as compared to typical CMOS and existing mixed logic design.

**Keywords:** This index includes such diverse concepts as Low power decoder, VLSI design styles, Gate Diffusion Input [GDI], Power efficiency.